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10/797,537

JRW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Rajesh S. Nair  
Serial No.: 10/797,537  
Filing Date: March 11, 2004  
Group Art Unit: 2822  
Examiner: Keisha L. Rose

Title: **HIGH VOLTAGE LATERAL FET STRUCTURE WITH IMPROVED ON RESISTANCE PERFORMANCE**

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450, Alexandria, VA 22313-1450, ON: September 7, 2005

Date of Deposit

Lydia McNamara SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.  
Name of Person Signing Certificate Name of Assignee  
Lydia McNamara 9/7/05  
SIGNATURE DATE

**SUBMITTAL OF FORMAL DRAWINGS**

Honorable Commissioner of Patents and Trademarks,  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Attn: Official Draftsperson**

SIR:

Enclosed are THREE (3) sheets of formal drawings for the above-identified patent application. The application was filed with informal drawings; please substitute the enclosed formal drawings for those currently on file. The formal drawing sheets are marked as "Replacement Sheets" in view of minor changes requested by Examiner Rose in an Office Action mailed to applicants on July 11, 2005.

Respectfully submitted,  
Rajesh S. Nair et al.

Kevin B. Jackson  
Attorney for Applicants  
Reg. No. 38,502  
Tel. (602) 244-5603  
Fax: (602) 244-3169

ON Semiconductor  
Law Dept./MD A700  
P.O. Box 62890  
Phoenix, AZ 85082-2890  
Attn: Lydia McNamara  
Date: September 7, 2005